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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/802,277	03/17/2004	Michael A. Halter	16990-52545-B	4213
7590	09/18/2008		EXAMINER	
J. Charles Dougherty Wright, Lindsey & Jennings LLP Suite 2300 200 West Capitol Avenue Little Rock, AR 72201			PHILOGENE, HAISSA	
			ART UNIT	PAPER NUMBER
			2821	
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			09/18/2008	PAPER

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

<b>Office Action Summary</b>	<b>Application No.</b>	<b>Applicant(s)</b>	
	10/802,277	HALTER, MICHAEL A.	
	<b>Examiner</b>	<b>Art Unit</b>	
	Haissa Philogene	2821	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

#### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

1) Responsive to communication(s) filed on 17 March 2004.  
 2a) This action is **FINAL**.                    2b) This action is non-final.  
 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

4) Claim(s) 1-26 is/are pending in the application.  
 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.  
 5) Claim(s) 24-26 is/are allowed.  
 6) Claim(s) 1-3,5-12,14-19 and 21-23 is/are rejected.  
 7) Claim(s) 4,13 and 20 is/are objected to.  
 8) Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

9) The specification is objected to by the Examiner.  
 10) The drawing(s) filed on 03 August 2004 is/are: a) accepted or b) objected to by the Examiner.  
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).  
 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
 a) All    b) Some \* c) None of:  
 1. Certified copies of the priority documents have been received.  
 2. Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.  
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

1) Notice of References Cited (PTO-892)  
 2) Notice of Draftsperson's Patent Drawing Review (PTO-948)  
 3) Information Disclosure Statement(s) (PTO/SB/08)  
 Paper No(s)/Mail Date 9/9/04.

4) Interview Summary (PTO-413)  
 Paper No(s)/Mail Date. \_\_\_\_\_.  
 5) Notice of Informal Patent Application  
 6) Other: \_\_\_\_\_.

## DETAILED ACTION

### ***Claim Objections***

Claims 10, 11 and 25 are objected to because of the following informalities: In claim 10, line 8, change “the” before “current” to –a—and in line 12, change “unit” after “calibration” to –circuit--. In claim 11, line 1, change “unit” after “calibration” to –circuit--.. In claim 25, line 1, change “a test fixture adapted” to –the step of adapting a test fixture—and in line 2, change “configured” to –configuring-- . Appropriate correction is required.

### ***Claim Rejections - 35 USC § 102***

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-3, 5-9, 19 and 21-23 are rejected under 35 U.S.C. 102(b) as being anticipated by Sherman, Patent No. 5,550362.

As per claims 1-3, 5-9, Sherman discloses in Fig.3D a lighting system, comprising:

(a) an LED (80); (b) a current regulator circuit (A8, Q1, R11) in communication with said LED; and (c) a calibration circuit (106) in communication with said current regulator; wherein said current regulator circuit comprises: (a) a drive unit (Q1) in series with said LED; (b) a current sensor (R11) in communication with said drive unit and said LED; (c) an adjusted voltage source (DAC unit) with an output OUT; and (d) a comparison unit (A8) in communication with said drive unit, said current sensor, and said adjusted voltage source wherein said comparison unit is operable to generate an

output to said drive unit that generates a voltage across said current sensor approximately equal to that of said output of said adjusted voltage source (see Col.17, lines 55-61); wherein said comparison unit (A8) is an operational amplifier. Sherman further discloses in Fig.3D a reference voltage source VREF, and wherein said adjusted voltage source (DAC unit) receives said reference voltage source as an input; wherein said adjusted voltage source is a digital-to-analog converter. Sherman further discloses a controller (96, see Fig.3B) in communication with said adjusted voltage source (DAC unit), and wherein said controller (96) is operable to send a (digital) signal to said adjusted voltage source via line (C) to modify said output of said adjusted voltage source; a storage unit (90, see Fig.3C) in communication with said controller (96) via line (B), wherein said storage unit (90) comprises calibration data and said controller (96) is operable to receive said calibration data from said storage unit (see Col.5, lines 7-8) and send said calibration data as digital signal to said adjusted voltage source via line (C) to modify said output of said adjusted voltage source; wherein said storage unit (90) is an EEPROM (see Fig.3C).

As per claims 19 and 21-23, Sherman discloses a method of controlling a lighting system comprising the steps of: (a) applying current to an LED (80) via current regulator circuit (A8, Q1, R11); (b) measuring the voltage across a current sensor (R11) in series with the LED via amplifier A8; (c) comparing via A8 the voltage across the current sensor with an adjusted reference voltage provided by DAC unit; and (d) emitting an electrical signal via A8 to a drive unit Q1 in series with the LED and the current sensor to cause the voltage across the current sensor to approximately equal the adjusted reference voltage (see Col.17, lines 56-61). 21. Sherman further discloses the step of generating the adjusted reference voltage via DAC (106) by modifying a reference voltage Vref based on a calibration value as digital signal on line C; wherein said step of generating the adjusted reference voltage is performed by a digital-to-analog converter (106), and further comprising the steps of: (a) emitting a digital signal via line C from a controller (96) to the converter (DAC), wherein the digital signal comprises an adjustment value readable as calibration data; and (b) transforming the digital signal comprising the adjustment value into an adjusted reference voltage by modifying the reference voltage by the adjustment value via DAC (106); further comprising the steps of: (a) storing the adjustment value in a storage unit

(90); and (b) reading said adjustment value from said storage unit to said controller (96) via line B.

***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 10-12 and 14-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sherman in view of Ducharme et al., Patent No. 7,014,336.

Sherman discloses in Figs. 3B-3D a lighting system comprising a calibration circuit (106, A8, Q1, R11) in communication with a LED (80), wherein said calibration circuit is operable to regulate a current applied to the LED in order to produce light from the LED of a standard temperature and intensity; and a controller (96) in communication with said calibration circuit via line (C); wherein said calibration circuit comprises: (a) a drive unit (Q1) in series with the LED; (b) a current sensor (R11) in communication with said drive unit and said LED; (c) an adjusted voltage source (DAC unit) with an output; and (d) a comparison unit (A8) in communication with said drive unit, said current sensor, and said adjusted voltage source wherein said comparison unit is operable to generate an output to said drive unit that generates a voltage across said corresponding current sensor approximately equal to that of said output of said corresponding adjusted voltage source (see Col.17, lines 55-61); wherein said comparison unit (A8) is an operational amplifier. Sherman further discloses in Fig.3D a reference voltage source VREF, and wherein said adjusted voltage source (DAC unit) receives said reference voltage source as an input; wherein said adjusted voltage source is a digital-to-analog converter. Sherman further discloses a controller (96, see Fig.3B) in communication with said adjusted voltage source (DAC unit), and wherein said controller (96) is operable to send a (digital) signal to said adjusted voltage source via line (C) to modify said output of said adjusted voltage source; a storage unit (90, see Fig.3C) in

communication with said controller (96) via line (B), wherein said storage unit (90) comprises calibration data and said controller (96) is operable to receive said calibration data from said storage unit (see Col.5, lines 7-8) and send said calibration data as digital signal to said adjusted voltage source via line (C) to modify said output of said adjusted voltage source; wherein said storage unit (90) is an EEPROM (see Fig.3C). Sherman does not disclose a plurality of LED arrays, wherein each of said LED arrays is operable to generate light of a distinct color, at least two of said LED arrays are operable to generate light of two distinct colors, and wherein said plurality of LED arrays are operable together to generate light of a spectrum of colors. However, these features are well known in the art as evidenced by Ducharme et al. which discloses in Figs. 2 and 3 a lighting system comprising a plurality of LED arrays (320), wherein each of said LED arrays is operable to generate light of a distinct color upon control by the processors (316), at least two of said LED arrays are operable to generate light of two distinct colors, and wherein said plurality of LED arrays are operable together to generate light of a spectrum of colors (see Col.9, lines 46-48 and 51-53 and Col.10, lines 7-11). It would have been obvious to a person having ordinary skill in the art at the time the invention was made to employ the plurality of LED arrays as taught by Ducharme into the Sherman type system, because it would ensure a calibration of the LEDs to generate high-quality light of a range of colors .

### ***Allowable Subject Matter***

Claims 4, 13 and 20 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims 24-26 are allowed.

### ***Conclusion***

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Vogel et al., Patent No. 6,759,814 ; Mueller et al., Patent No. 7,344,279.

***Correspondence***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Haissa Philogene whose telephone number is (571) 272-1827. The examiner can normally be reached on 8:30 A.M.-6:00 P.M..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Douglas W. Owens can be reached on (571)272-1662. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/H. P./

/Haissa Philogene/  
Primary Examiner, Art Unit 2821

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